A MONOLITHIC MONOPULSE COMPARATOR

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ABSTRACT

A GaAs monolithic monopulse comparator operating at L-band has been developed. The complete circuit is composed of four summing amplifiers and four difference amplifiers. The circuit has a gain of 8.5 dB, null depths of ~ 25 dB to 30 dB, and is biased from a single positive supply. This is the first monolithic monopulse comparator circuit to have been demonstrated.

INTRODUCTION

Great strides have been made over the past decade to advance the state-of-the-art in GaAs MMIC design. LNAs, power amplifiers, mixers, switches, phase shifters, and attenuators are some of the circuit functions which have received considerable attention. These, in turn, have been used to form higher levels of integration with functions such as high gain transmit modules, downconverters, and transmit/receive modules.

This paper describes a new application of MMICs, summing and difference amplifiers, and their integration into a microwave monolithic monopulse comparator for use in monopulse radars.

Summing (Σ) Amplifier

A schematic diagram, Figure 1, shows the topology of the circuit. The 3 dB gain requirement is lower than typically desired for microwave amplifiers, and therefore lossy elements were used in the matching networks to reduce the gain. Series inductive feedback was also used in this design to improve the input match, reduce the noise figure, and reduce the gain. The choice of FET periphery was driven by the third order intercept requirement. The 200 μm FET was the smallest one which allowed the 17 dBm IP3 goal to be met.

The FET is self-biased with a source resistor. Bias was supplied through an on-chip spiral inductor with capacitive by-passing at the bias port. Therefore, this circuit did not require any additional circuitry to operate.

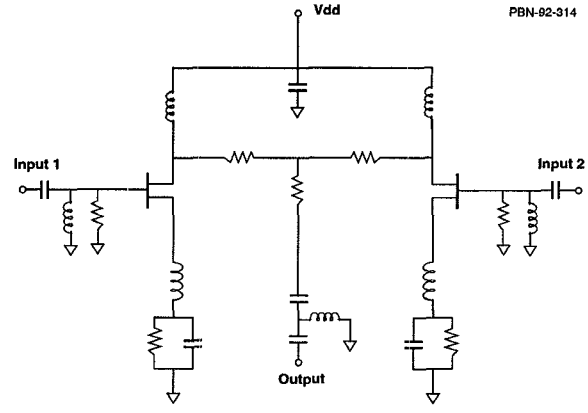

Figure 1. Schematic Diagram of Summing Amplifier.

Difference (Δ) Amplifier

One of the most critical performance specifications for the Δ amplifier is a Common Mode Rejection Ratio (CMRR) of greater than 35 dB in order to meet the receiver null depth specification. Yet a single Δ amplifier is simulated to have a CMRR of about 15 dB.

Several methods were considered to improve CMRR. The first used a passive balun to provide a single-ended output from the differential output of the circuit. This was rejected because the size of the circuit would be prohibitive at L-band. Another approach formed an active balun with a common-source and a common-gate FET pair. The disadvantage with this approach was that nulling was sensitive to the amplitude balance, and the circuit did not maintain good balance over temperature.

The chosen approach used a second Δ amplifier as a balun. The circuit was, therefore, composed of a Δ amplifier stage whose Δ output was fed into the input of a second Δ amplifier stage. The CMRR, taken as single-ended output from this second stage, was simulated to be 44 dB.

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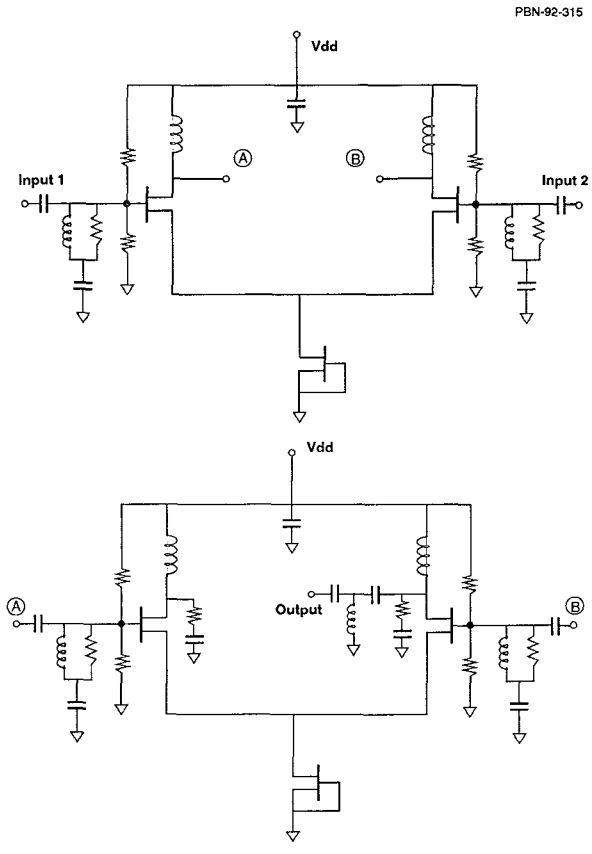

Figure 2. Schematic Diagram of Difference Amplifier.

The schematic diagram of this circuit is shown in Figure 2. This design's FET periphery used in this design was the largest one allowed so that the input to input isolation requirement could be met. The isolation is more of a problem in the Δ amplifier than the Σ amplifier since the former couples through the gate-source capacitance, while the latter couples through the gate-drain capacitance. Typically C_{gs} is an order of magnitude larger than C_{dg}.

Lossy matching was also used in this circuit to reduce the gain to the specified level.

Inductors, resistors, and active loads were considered for the load. The dc voltage drop across a resistive load was far too large. An active load would provide a high resistance, a moderate voltage drop, and a relatively small size, but biasing three FETs in series was considered a risky approach. Therefore, inductors were chosen even though at 2 GHz this element is large.

The entire circuit is self-biasing. Bias is supplied through an on-chip spiral inductor with capacitive by-passing at the bias port. As with the Σ amplifier, the Δ amplifier required no external components.

Circuit Layout

Special care was taken in the layout of the Σ and Δ amplifiers to maintain symmetry between the RF inputs and the point where the circuits become single-ended as the chip photos in Figures 3 and 4 illustrate. The asymmetry seen in the layout of the output matching networks and the bias networks have no bearing on the circuit performance. Bias can be supplied from either side of the chips. This is especially important in the Σ and Δ circuits to make biasing the full monopulse chip more convenient.

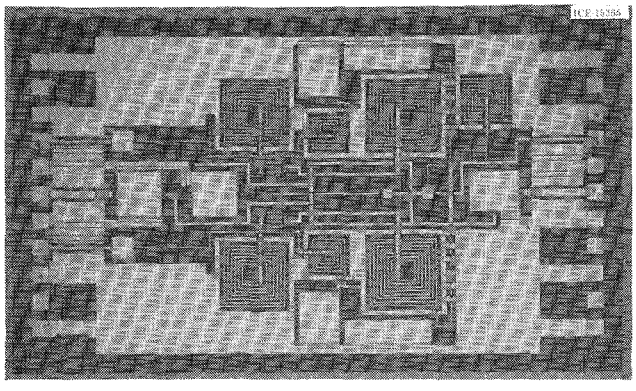

Figure 3. Photograph of a Summing Amplifier.

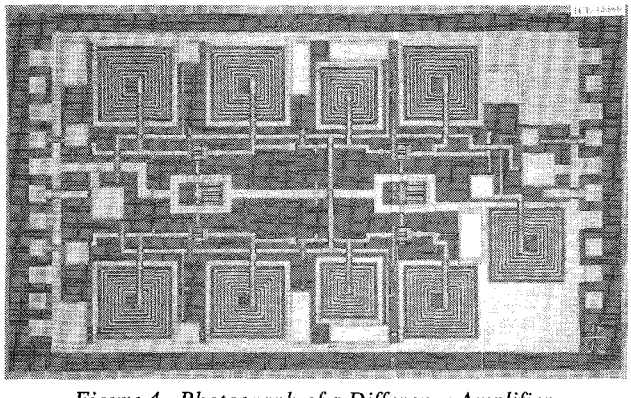

Figure 4. Photograph of a Difference Amplifier.

The monopulse circuit, shown in Figure 5, is composed of four Σ and four Δ amplifiers. The lines interconnecting these circuits were carefully laid out such that the phase length of the signal pairs feeding each of the four output circuits are equal. The size of this chip is 302 mils by 292 mils.

Fabrication

The circuits were fabricated using a pocket implant process. The gates were aligned to the n+ implant mask to allow accurate positioning of the gate between the n+ contacts, allowing heavily doped contacts to be implanted, reducing the "on" resistance, and allowing the circuits to operate at a low supply voltage.

The remainder of the process used standard MMIC fabrication techniques, providing 2000Å SiNx MIM capacitors, TaNx thin film resistors, interconnects, and air bridges. These circuits have no via holes or back-side metalization, and the substrate thickness is 25 mils.

Measured Results

Standard G-S-G probes were used to measure the circuit. Two-port measurements were made, leaving the remaining RF ports floating. This gave an adequate measure of the operation of the circuits under actual operation since the inputs have at least 20 dB of isolation between them.

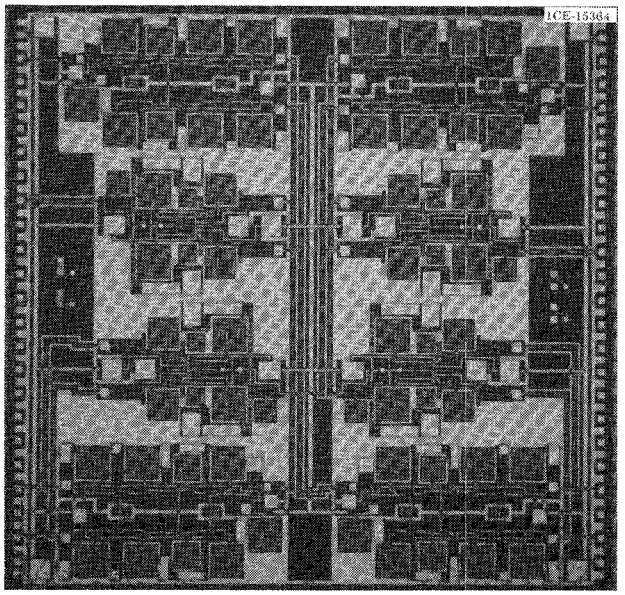

Figure 5. Photograph of a Monopulse Comparator.

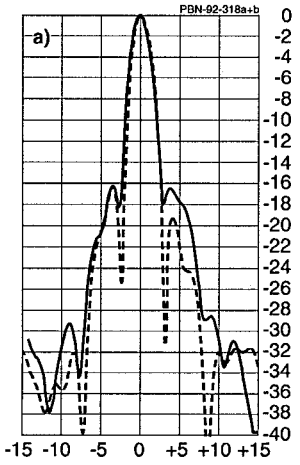

Figure 6a. Antenna Patterns of Monopulse Review, Σ Channel Output Scanned in Elevation and Azimuth.

Monopulse Comparator Circuit

Since this is an 8-port circuit, six ports were left floating, and a total of 16 sets of two-port S-parameters were measured to characterize each circuit. The S-parameter data was then entered into a spreadsheet program to analyze how the circuit would perform at each output port if signals were simultaneously present at more than one input. This was used to estimate the null depth provided by the monopulse circuit. With signals equal in amplitude and phase present at all four inputs (boresight condition), the gain referenced to a single input was typically 8.5 dB at the sum port. The corresponding null depths at the elevation, azimuth, and fourth output ports were -25, -27, and -33.4 dB, respectively. The null depth is approximately equal to the CMRR of the Δ amplifier.

The monopulse circuit was assembled into a monopulse receiver. Patterns measured at the Σ channel output as the antenna is scanned in elevation and azimuth are shown in Figure 6a. Patterns measured in the elevation and azimuth channels are shown in Figure 6b. The patterns clearly demonstrate the operation of the monopulse circuit.

CONCLUSION

A GaAs monolithic monopulse comparator operating at L-band has been developed. Significant size reductions have been realized compared to passive monopulse circuits operating at the same frequency. This is the first MMIC of its type to be demonstrated.

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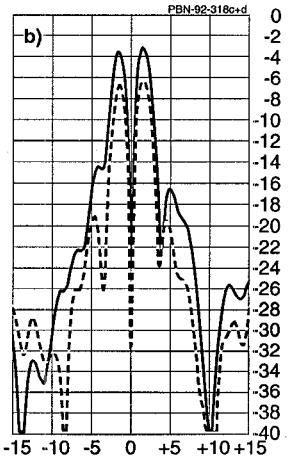

Figure 6b. ΔEl Channel Scanned in Elevation, and ΔAz Channel Output Scanned in Azimuth.